AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A flip-flop comprising:
   a. a differential output stage having differential first and second input terminals and complementary first and second output terminals;
   b. a transistor having a first current-handling terminal connected to the first output terminal, a second current-handling terminal connected to the second output terminal, and a control terminal;
   c. wherein the differential output stage includes, a cross coupled circuit having a cross coupled transistor configured to continuously receive power from a positive power supply voltage, wherein a gate of the cross coupled transistor is connected to the second output terminal;
   d. a differential input stage having differential third and fourth input terminals and complementary third and fourth output terminals connected to the first and second input terminals, respectively; and
   ~~e.~~ wherein the differential input stage includes, another transistor having a current-handling terminal continuously connected to VSS and a gate connected to the third input terminal~~;~~, and ~~—~~
   ~~f.~~ another cross coupled circuit including another cross coupled transistor having a gate connected to the fourth output terminal.

2. (Original) The flip-flop of claim 1, further comprising a clock terminal connected to the control terminal.

3. (Original) The flip-flop of claim 1, further comprising a second transistor having a third current-handling terminal connected to the first input terminal, a fourth current-handling terminal connected to the second input terminal, and a second control terminal.

4. (Previously Presented) The flip-flop of claim 3, further comprising a first clock terminal connected to the first-mentioned control terminal and a second clock terminal connected to the second control terminal.

5. (Original) The flip-flop of claim 4, wherein the first and second clock terminals are adapted to receive complementary clock signals.

Claims 6-9 (Cancelled)

10. (Currently Amended) A flip-flop comprising a differential input stage having differential first and second input terminals, differential third and fourth input terminals, a first transistor, and complementary first and second output terminals, wherein the first transistor has a first control terminal connected to the first input terminal and a current handling terminal directly connected to VSS, and further comprising another transistor having a first current-handling terminal connected to the first output terminal, a second current-handling terminal connected to the second output terminal, and a control terminal receiving a clock signal and further comprising a cross coupled circuit having a cross coupled transistor directly connected to a positive power supply voltage, wherein a gate of the cross coupled transistor is connected to the second output terminal.

11. (Previously Presented) The flip-flop of claim 10, wherein the input stage further comprises a first leg including the first transistor and a second transistor connected in parallel, the second transistor having a second control terminal connected to the third input terminal.

12. (Original) The flip-flop of claim 11, wherein the input stage further comprises a second leg including third and fourth transistors connected in series, the third transistor having a third control signal connected to the second input terminal and the fourth transistor having a fourth control terminal connected to the fourth input terminal.

Claims 13-14 (Cancelled)

15. (Previously Presented) The flip-flop of claim 10, further comprising an output stage having:
    a. differential fifth and sixth input terminals connected to respective ones of the first and second output terminals;
    b. complementary third and fourth output terminals; and
    c. a transistor having a first current-handling terminal connected to the third output terminal, a second current-handling terminal connected to the fourth output terminal, and a second control terminal.

16. (Previously Presented) The flip-flop of claim 15, further comprising a clock terminal connected to the second control terminal.

17. (Previously Presented) A counter circuit comprising:
    a. a first flip-flop having:
        i. a differential output stage having differential first and second input terminals and complementary first and second output terminals; and
        ii. a first transistor having a first current-handling terminal connected to the first output terminal, a second current-handling terminal connected to the second output terminal, and a first control terminal; and

iii. a cross coupled circuit having a cross coupled transistor directly connected to a positive power supply voltage, wherein a gate of the cross coupled transistor is connected to the second output terminal; and

b. a second flip-flop having:

i. a differential input stage having differential third and fourth input terminals connected to the respective first and second output terminals of the first flip-flop, a second transistor, and complementary third and fourth output terminals, the second transistor having a gate connected to the third input terminal and a current handling terminal directly connected to VSS; and

ii. a third transistor having a third current-handling terminal connected to the third output terminal, a fourth current-handling terminal connected to the fourth output terminal, and a second control terminal.

18. (Original) The counter of claim 17, wherein the first and second control terminals are adapted to receive complementary clock signals.

19. (Original) The counter of claim 17, the first flip-flop further comprising a second differential input stage having differential fifth and sixth input terminals and complementary fifth and sixth output terminals, wherein the fifth and sixth output terminals are connected to the first and second input terminals, respectively.

20. (Original) The counter of claim 17, the second flip-flop further comprising a second differential output stage having differential fifth and sixth input terminals connected to the third and fourth output terminals, respectively.